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Scientific Research

Design and Implementation of Double Base Integer Encoder of Term Metrical to Direct Binary Code Application

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ABSTRACT

The digital processing signal is one of the subdivisions of the analog digital converter interface; data transfer rate in modern telecommunications is a critical parameter. The greatest feature of parallel conversion rate (4-bit parallel Flash 5/s converter) is designed and modeled in 0.18 micron CMOS technology. Low speed swing operation as analog and digital circuits leads to high speed of low power operation power with 70 mVt 1.8 V A/D converter from the power dissipated during operation in the 5 GHz range. Average offset is used to minimize the effect of the bias of a comparator. This paper contains the 8-bit encoder of the metrical term code to direct binary code decreasing power consumption, which is shown by results and comparison with other designs using computer simulation. The results of the flash ADC time-interleaved are a more significant improvement in terms of power and areas than those previously reported.

Keywords: ADC; CMOS VLSI; High Speed Data Converters; Code

1. Introduction

Digital communication tools with high data rate, high speed broadband, radar and optical communications, these applications require 4 to 6 bit resolution at rates of 1 GHz or beyond.

Several papers have been published previously in the 4-bit Flash ADC [1]. The multi-GHz A/D sampling rate is achieved by using interleaved time architecture.

Because of the gain and offset of the inconsistencies among the various channels of ADC time-interleaved architecture usually requires numerical methods [2].

These calibrations scheme to significantly increase the power and/or Flash ADC area. The proposed architecture 5/s speed is achieved based on low swing in full operation of the ADC. Two stages on average bias resistor give relations in 3.65.

Thus no digital calibration is required, encoding to significant savings in power and scope.

Resistor ladder generates tap voltage 21 voltage references from two clean 0.9 V and 1.6 V. 21 multi-stage comparators, including 15 major and over-3 range comparators on each end of the array, compare the input signal voltage from the crane and generate code thermometer. Finally, the current encoder mode logic (CML) translates the code with binary thermometer through the intermediate gray code [3,4].

No external track and hold (t/h) is used in the ADC. Instead, the sample is distributed in the first latch comparator array.

2. Comparator Array

Preamplifier an array is a regenerative latch that operates as a distributed monitor and keep, and two additional tabs are available to achieve further enhancement and differential swing low level in the comparators' output [5]. No hours available for preamp which gives a continuous signal to the first latch. Shows the schematic of the preamplifier to **Figure 1**.

Related Works

Development of Eight-Encoder Design Steps

Inputs to the capacity of the output code from four to eight digits are based encoders lower order Exam.

The XOR Gate schematic CML shows after piping the propagation delay of the slow pipeline stage limits the

operating frequency. So to implement an efficient scheme of piping, it is desirable to have some delays at all stages [6].

Diagram of the encoder is shown in **Figure 2** and developed in accordance with prudent use of a minimum number of components, which reduces the space occupied by the on-chip. MOSFETs-substrate transistors with n-channel T_1, T_4 and T_5 are connected to the negative rail power supply Vss, and the substrate p-MOSFETs with channel T_2, T_3 and T_6 to the positive rail Vdd [7].

Encoder (**Figure 2**) consists of two CMOS—keys on the basis of transistors T_1, T_2 and T_5, T_6, which are controlled by the voltage at the input X_1; Y_0 determines the MSB output binary code. Input X_1 comes from the output of the comparator switching threshold which corresponds to the middle of the two-digit range input ADC. Keys at the same switching voltage X_0 and X_2 from the outputs of the other two comparators to generate low-order output Y_1 binary ADC. Based on the proposed scheme can be implemented three-bit encoder, where a block with two-digit designation DEC encoder according Proceeding similarly, we obtain a four-digit encoder circuit based on the three-digit encoder [8]. This requires the use of two-input multiplexers labeled MUX, **Figure 3** shows its' scheme. Substrate MOSFET with n-channel T_2, T_4, T_5, T_6, T_8 and T_{10} are connected to the negative rail power supply V_{ss}, and the substrate MOSFETs p-channel T_1, T_3, T_7 and T_9—to the positive rail V_{dd}. The multiplexer is a signal at the address input A. When the signal at input A, equal logical unit, the output signal from the input D_1, and when the signal A, equal to a logical zero, with input D_2. Inverters based on transistors T_7 - T_{10} are the buffer elements. Thus, increasing the bit similar to **Figure 3**.

Modeling was conducted with (tt, ss, ff, snfp, fnsp) for three values of temperatures −40˚C and 27˚C, 85˚C. The

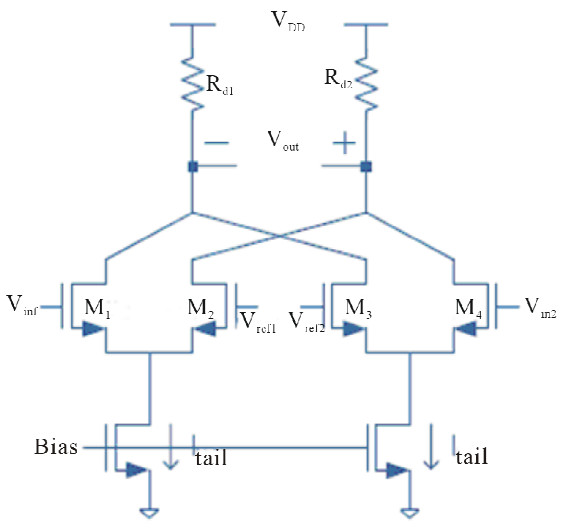

Figure 1. Schematic of the preamplifier.

results are presented in **Table 1**.

3. Material and Methods Simulation Results

Power characteristics of the encoder performed using MOSFETs Cadence Virtuoso based on 180 nm CMOS technology from UMC to 1.8 V single supply [9]. Delay time-shift eight-evaluated by the response of the encoder output LSB Y8 direct binary code when the input code in the thermometric all 255 bits of logic zero to logic one on the front, and vice versa trailing edge, due to the encoder circuit solution. According to the presented in the previous section schemes, the most time-delay switch will have LSB output direct binary code. Clock frequency. Winning on the power consumption of circuit solutions presented encoder compared to known analogs [8-10] can evaluate on the basis of the simulation results. It is necessary to implement the conversion of power consumption being compared encoder (P_{ref}) the equivalent Encoder, executed in the same way, 8-bit word length, manufactured in 180 nm CMOS technology and has a clock speed of 1 GHz. In this case, the supply current from the translation were held constant. Then the change in power consumption can be estimated: at another bit by the coefficient [9].

$N_{eq} - N_{ref}$ bit Equivalent, and compares the encoder respectively, when changing technology—a factor $\frac{E_e}{E_c}$.

E_{eq}—voltage encoder, made in 180 nm CMOS technology $\left(E_{eq} = 1.8\ \text{B}\right)$, E_{ref}—encoder supply voltage being compared; when the clock—$\frac{F_e}{F_c}$, F_{eq} & F_{ref}—clock frequency equivalent to the developed and the compared encoders respectively. Then the equivalent power consumption is defined as

$$F_{eq} = 2^{N_{eq}-N_{ref}}\, p_{ref}\, \frac{E_{eq}}{E_{ref}} \frac{F_{eq}}{F_{ref}}.$$

Table 2 under the conditions of winning based on estimates of power consumption circuitry solutions developed encoder compared to known analogs is table.

The minimal gain in power consumption is obtained for eight-ADC encoder from Gain in power consumption is obtained for eight-ADC encoder from [10]

$$\frac{P_{eq}}{P_{dev}} = \frac{0.438}{0.439} \frac{1.8}{0.7} \frac{1}{2} = 1.3\ \text{T}$$

P_t—average power consumption of the developed encoder. The maximum gain in power consumption is obtained for the encoder [11] on the basis of multiplexers.

$$\frac{P_{eq}}{P_{dev}} = \frac{0.254}{0.449} \frac{1}{0.1} = 45.3\ \text{T}$$

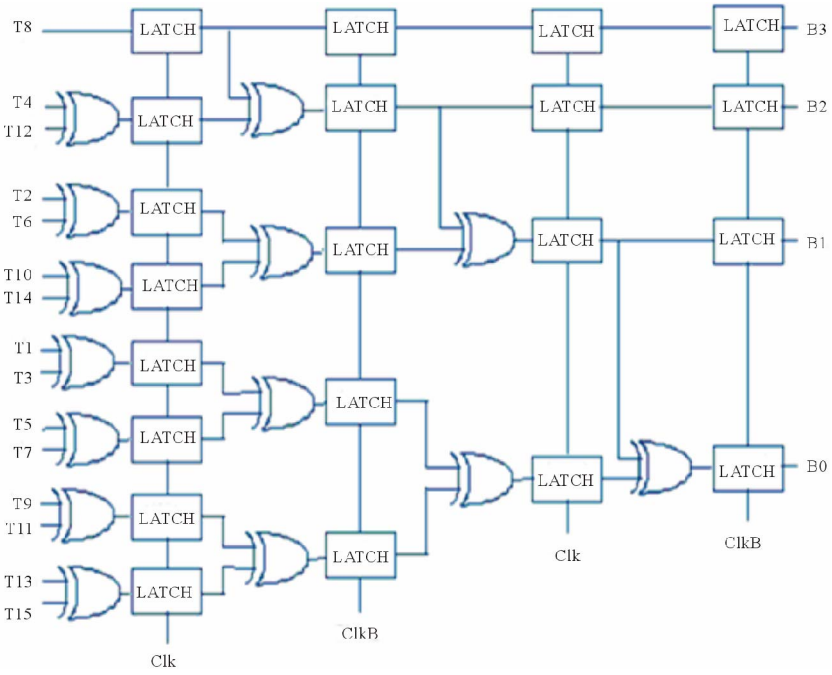

Figure 2. Implementation of encoder with four stage pipeline and only one type of gate.

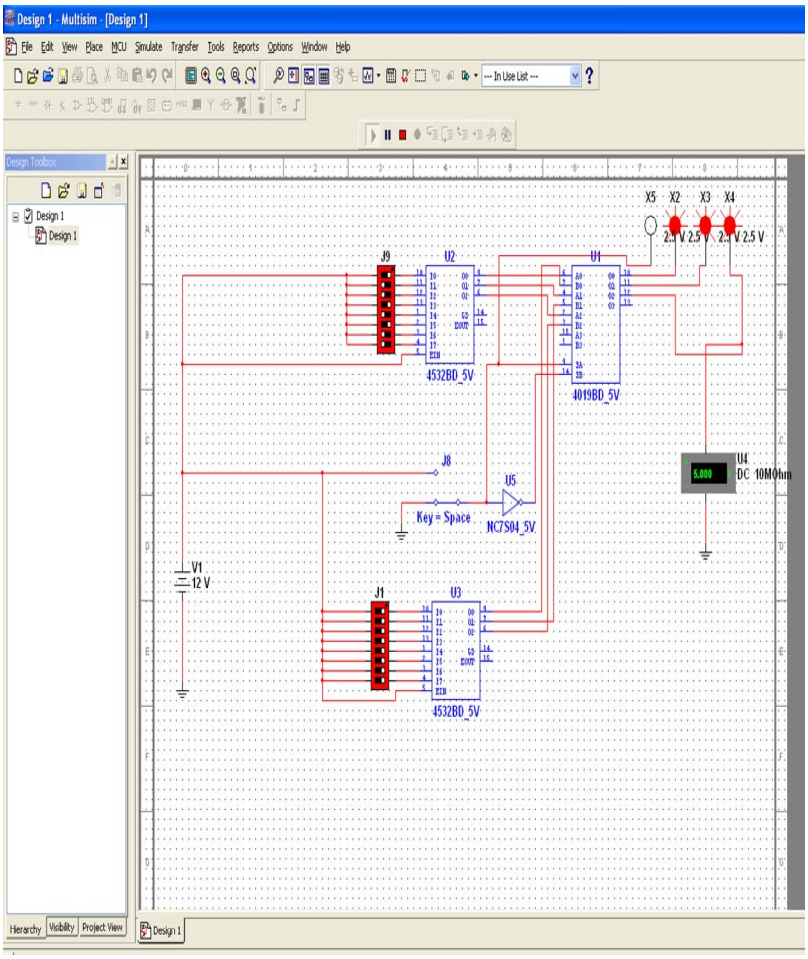

Figure 3. Eight-bit encoder.

Table 1. Consumption of the encoder.

Terms	T ˚C	*Time-delay switch*	*Duration of the recession*	*Front time*	*Power consumption*
	−40	584	24	43	430
tt	27	640	29	50	442
	85	689	32	55	461
	−40	881	31	59	411
ss	27	957	38	70	429
	85	1020	44	78	446
	−40	431	19	33	446
ff	27	475	23	39	460
	85	513	26	43	485
	−40	666	24	44	469
snfp	27	726	29	51	483
	85	778	34	56	504
	−40	434	24	45	408
Snsp	27	588	28	52	425
	85	634	23	58	443
Mean value		674	29	52	449
The maximum value		1020	44	78	504

Table 2. Decreased power consumption.

Encoder	CMOS	Power consumption. (t)
Full Adders	**0.18**	**24.7**
Memory Elements		**41.6**
Multiplexers		**45.2**
Logic Elements		**1.4**

4. Conclusion

The paper proposed a circuit solution to thermometric encoder code in straight binary code. Eight-circuit simulation performed in CAD Cadence Virtuoso for 180 nm CMOS technology with a unipolar voltage 1.8 V. Maximumly delayed time-shift is about 1 ns, which allows the use of the scheme in the processing of signals with a frequency of 1 GHz along with existing analogues. Average power consumption does not exceed 500 mW. All else being equal to a gain on the power consumption in comparison, the known digital calibration can be added to implement ultra-high-speed time-interleaved ADCs to 40 times. The reduction in the number of comparators architecture makes it useful in portable ECG systems which operate at low voltage and low frequency range.

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